What is claimed is:

1. An infrared sensing device, comprising:

semiconductor substrate having a face;

readout integrated circuit formed at said face of said semiconductor substrate;

a mesa of Group II - VI semiconductor material formed on said face of said semiconductor substrate;

at least one planar photovoltaic infrared detecting cell formed in said mesa; and

a conductor interconnect layer monolithically connecting said infrared detecting cell to said readout integrated circuit.

2. The infrared sensing device according to claim 1, wherein:

said conductor interconnect layer monolithically connects a common contact cell of said photovoltaic infrared detecting cell lying in one plane to a readout integrated circuit common contact cell lying in another plane, the two planes being separated by a height difference of more than 15 microns.

3. The infrared sensing device according to claim 1, wherein:

said mesa includes at least two layers of Group II - VI semiconductor material having different band gaps, and

at least one p-n junction diode of said infrared detecting cell being formed in one of said two layers of Group II-VI semiconductor material.

4. The infrared sensing device according to claim 1, further comprising:

a detector output conductively connected to said readout circuit input cell;

a detector common conductively connected to said readout circuit common cell;

said mesa having at least one sloped side; and

at least one conductive trace formed on said sloped side connecting said detector output and said first input of said readout integrated circuit.

5. The infrared sensing device according to claim 3, wherein said sloped side of said mesa has a slope angle between about 40 and 50 degrees relative to a horizontal plane.

6. An Infrared sensing device, comprising:

a readout integrated circuit fabricated on a substrate having a one degree tilt from a (100) crystal direction; and

a mesa formed on said readout integrated circuit, said mesa including:

a buffer layer;

a first layer of Group II - VI semiconductor material having a first band gap on said buffer layer;

said buffer layer functionally reducing mismatch between said readout integrated circuit and said first layer of Group II - VI semiconductor material;

a second layer of Group II - VI semiconductor material disposed on said first layer of Group II - VI semiconductor material, said second layer of Group II VI semiconductor material having a second band gap different from said first band gap;

first and second rows of infrared detecting cells,

said first row of infrared detecting cells conductively connected to a first row of signal input gates of said readout circuit; and

said second row of infrared detecting cells conductively connected to a second row of signal input gates of said readout circuit.

7. The Infrared sensing device according to claim 6, wherein said first layer of Group II - VI semiconductor material is formed of indium doped n-type HgCdTe.

8. The Infrared sensing device according to claim 6, wherein the said second layer of Group II - VI semiconductor material is formed of indium doped n-type HgCdTe with a band gap larger than the said first n-type HgCdTe layer.

9. The Infrared sensing device according to claim 6, wherein said first and second rows of infrared detecting cells include an arsenic compound at least partially extending into said first layer of Group II - VI semiconductor material layer.

10. An Infrared sensing device having at least one infrared light sensitive element, comprising:

a readout integrated circuit formed at a face of a semiconductor layer having a tilt of approximately one degree from the (100) crystal direction;

a mesa formed on a first surface of said readout integrated circuit, said mesa including:

buffer layer;

a first layer of Group II - VI semiconductor material on said buffer layer, said first layer of Group II - VI semiconductor material having a first band gap;

said buffer layer functionally reducing mismatch between said readout integrated circuit and said first layer of Group II - VI semiconductor material;

a second layer of Group II - VI semiconductor material disposed on said first layer of Group II - VI semiconductor material, said second layer of Group II -VI semiconductor material having a second band gap; and

said first band gap being different from said second band gap.

11. A monolithic infrared detector array according to claim 10, further comprising:

a first infrared detecting cell at least partially extending into said first layer of Group II - VI semiconductor material;

a second infrared detecting cell at least partially extending into said first layer of Group II - VI semiconductor material, said second infrared detecting cell not overlapping said first infrared detecting cell;

a first conductive interconnect trace formed between said first infrared detecting cell and signal input gates of said readout circuit,

a second conductive interconnect trace formed between said second infrared detecting cell and signal input gates of said readout circuit,

said mesa having first and second sloped sides;

said first conductive interconnect trace running over said first sloped side of said mesa;

said second conductive interconnect trace running over said second sloped side of said mesa.

12. A method for fabricating a monolithic infrared detector, comprising the steps of:

a) providing on a read-out integrated circuit a Si(001) surface;

b) etching the Si(001) surface to yield a dyhdride terminated smooth Si(001) surface;

c) inserting the read-out integrated circuit and clean and passivated Si(001) surface into an MBE chamber;

d) growing a buffer layer of single crystalline CdTe on the ROIC within the MBE chamber while maintaining the ROIC at a temperature less than 500 degrees C;

e) depositing within the same MBE chamber a first layer of HgCdTe with narrow band gap on the buffer layer within the MBE chamber while maintaining the ROIC at a temperature less than 500 degrees C; and

f) depositing within the same MBE chamber a second HgCdTe layer with a relatively wider band gap on the first layer of HgCdTe within the MBE chamber while maintaining the ROIC at a temperature less than 500 degrees C.

13. The method of claim 12, wherein the step of etching comprises the steps of:

b-1) etching the Si wafer in a diluted solution of HF:H_20 to remove the passivation layer; and

b-2) etching the Si wafer in a concentrated solution of NH_4F to yield a dyhdride terminated smooth Si(001) surface.

14. The method of claim 12, further comprising the steps of:

g) depositing a thin CdTe cap layer on the second HgCdTe layer;

h) coating the entire structure with a photoresist;

i) selectively opening a plurality of windows in the photoresist;

j) fabricating a plurality of p-n junctions by implementing arsenic atoms through the windows selectively by ion implantation technique;

k) annealing the ROIC to activate the arsenic;

l) removing the masking photoresist layer;

m) selectively protecting the grown infrared material structure with a photoresist while leaving the remaining areas uncovered;

n) etching the uncovered areas to expose the ROIC contact pads;

o) selectively protecting the grown infrared material structure with a photoresist, leaving the rest of the areas open; and

p) etching the entire sample to produce a mesa structure with a 40 to 50 degree angle between the mesa side walls and horizontal plane.

15. The method of claim 14, wherein a solution of 4% bromine in hydrobromic acid solution is used in the step of etching to produce a mesa structure.